Industry Standard Control Interfaces for inter IC Communication

Moritz Nöltner

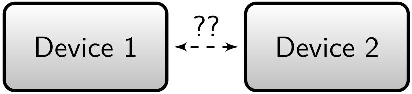
Institut für Technische Informatik
Lehrstuhl für Rechnerarchitektur
Universität Heidelberg

January 28, 2015

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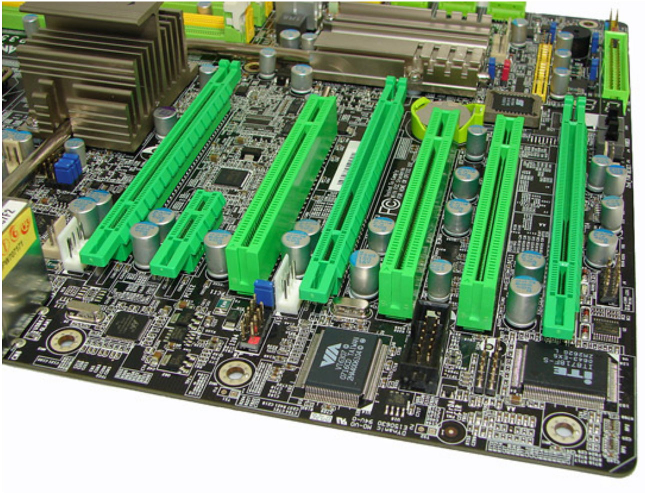
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How to Connect Circuits?



- HyperTransport
- PATA, SATA
- PCI, PCI-Express
- AGP
- ISA
- USB
- CAN
- UART, USART
- SPI
- I²C, SMBus
- UNI/O
- 1-Wire

Speed <=> Simplicity



Source: `http://www.anandtech.com/show/2354/2`

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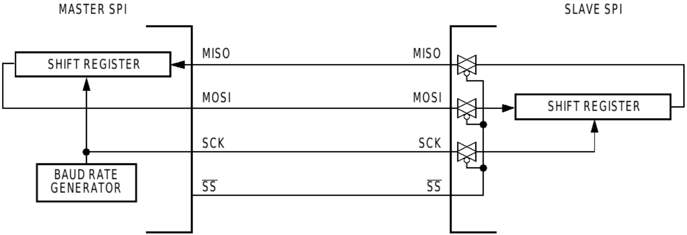
Serial Peripheral Interface



Source: http://en.wikipedia.org/wiki/File:Motorola_MC6800_microprocessor.jpg

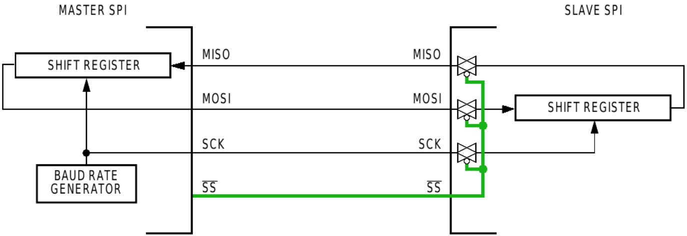
- Created in the 1980s
- First used in Motorola 6800
- Very widely accepted
- Bus system
- Full duplex
- Four signal lines typically

SPI Signal Lines



Source: Adapted from ``SPI Block Guide V 03.06'', 2003

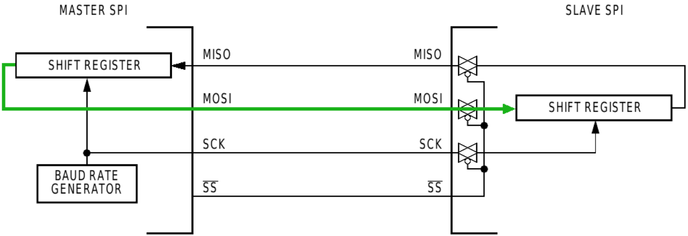
SPI Signal Lines



Source: Adapted from ``SPI Block Guide V 03.06'', 2003

- SS — Slave Select
  Slaves will only interact if their SS is acrive

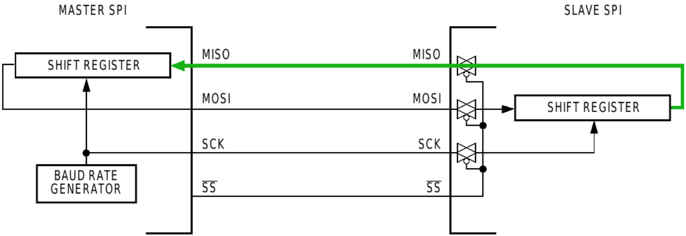
SPI Signal Lines



Source: Adapted from ``SPI Block Guide V 03.06'', 2003

- MOSI — Master Out, Slave In
  Serial data line for master to slave

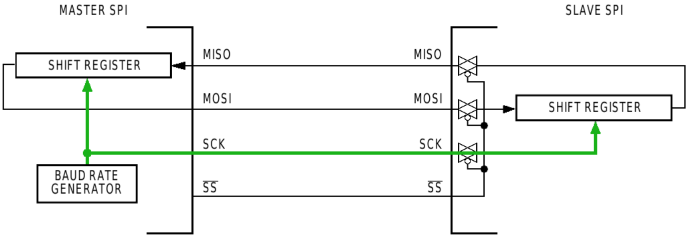
SPI Signal Lines



Source: Adapted from ``SPI Block Guide V 03.06'', 2003

- `MISO` Master In, Slave Out
  Serial data line for master to slave

SPI Signal Lines

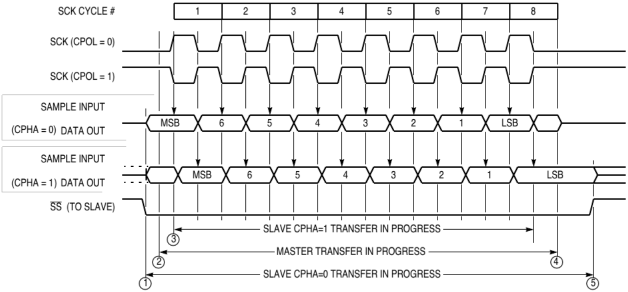


Source: Adapted from ``SPI Block Guide V 03.06'', 2003

- CLOCK — Shift Clock
  One bit is sent per clock cycle

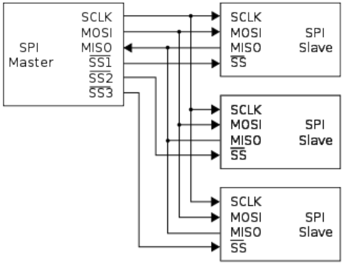
Clock Phase & Polarity

4 combinations:



Source: Taken from the datasheet for Motorola MC68HC11A0

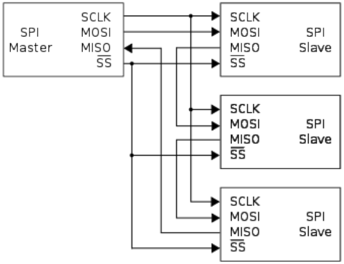
SPI Bus Topologies: Star



Source: Adapted from http://en.wikipedia.org/wiki/File:SPI_three_slaves.svg

- 3+n signal lines
- `MOSI`, `MISO`, `CLOCK` shared
- One `SS` for every slave
- Master activates a slave and communicates with it
- No delay

SPI Bus Topologies: Serial

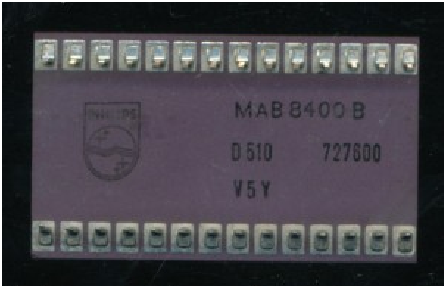


Source: Adapted from http://en.wikipedia.org/wiki/File:SPI_three_slaves_daisy_chained.svg

- Four signal lines
- MOSI, MISO, CLOCK, SS shared
- Messages are passed through
- Messages get latched, when SS is deasserted
- Not supported by all devices
- Delayed responses, message has to pass adjacent slaves

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Inter-Integrated Circuit



Source:
http://www.cpushack.com/gallery-1/philips/philipsmab8400b

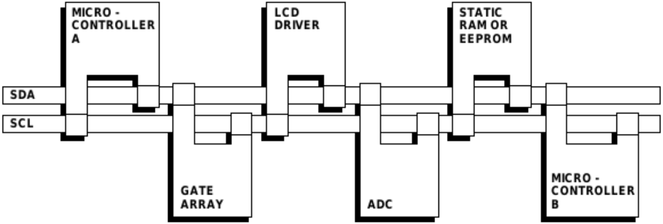
- Created in the 1980s
- First used in Philips MAB8400B
- Very widely accepted
- Compatible with other buses: SMBus, PMBus
- Bus system
- Multi-master operation
- Half duplex (simplex)
- Two signal lines + two pull-up resistors

I^2C Roles

Four roles possible:

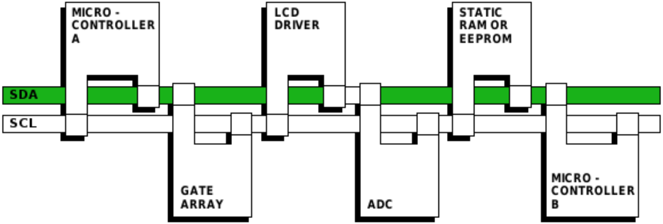
▪ Master	Starts a transmission
▪ Slave	Responds to transmission
▪ Transmitter	Transmits data
▪ Receiver	Receives data

I^2C Signal Lines



Source: Adapted from ``The I^2C-Bus Specification v. 2.1'', 2000

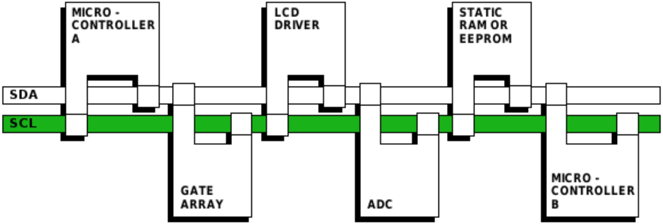
I^2C Signal Lines



Source: Adapted from ``The I²C-Bus Specification v. 2.1'', 2000

- SDA — Seria Data
  Bidirectional data– & address line

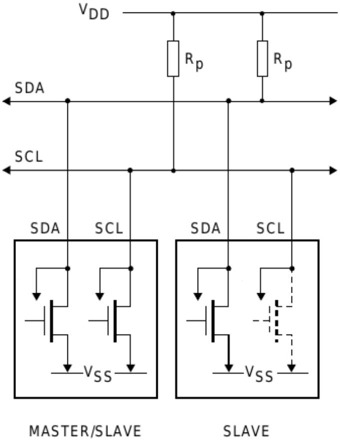
I^2C Signal Lines



Source: Adapted from ``The I^{2}C-Bus Specification v. 2.1'', 2000

- SCL — Serial Clock
  Used by the master to synchronise with the slaves

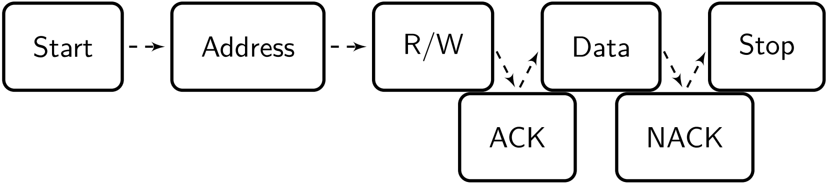
I^{2}C Electrical Setup



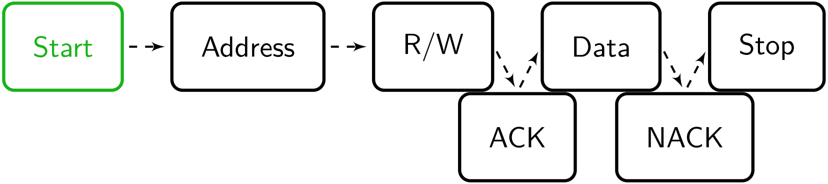
Source: Adapted from ``The I^{2}C-Bus Specification v. 2.1'', 2000

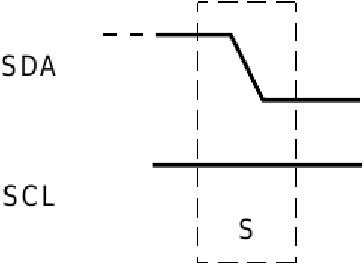
- Open-drain or open-collector outputs
- Wired-AND

I²C Protocol Parts



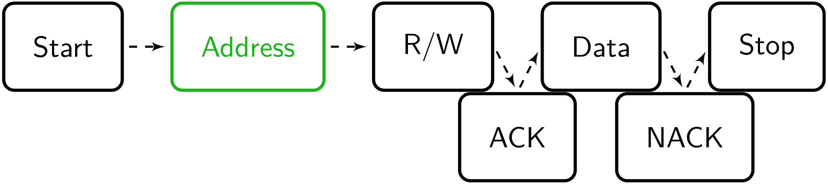
I²C Protocol Parts





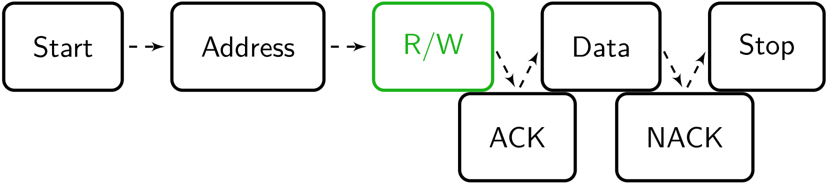
- SCL high
- Master injects negative Edge on SDA

I^{2}C Protocol Parts



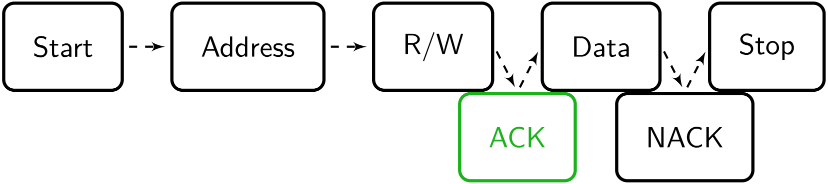
- Seven bits of address are transmitted
- Some addresses are reserved

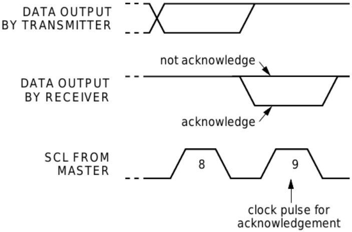
I²C Protocol Parts



- "1" for reading
- "0" for writing

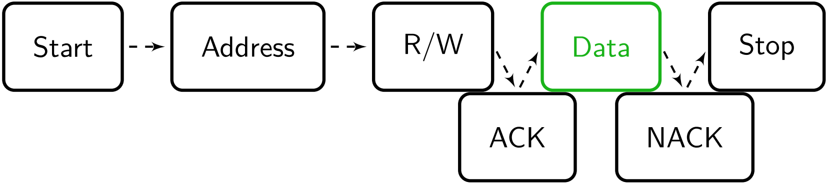
I²C Protocol Parts





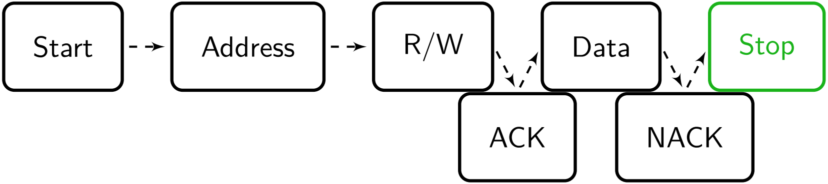
- Transmitter releases the SDA line
- Receiver pulls SDA low to acknowledge

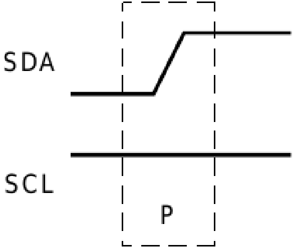
I²C Protocol Parts



- Transmitter sends one byte of data
- It may send the next byte if receiver acknowledges
- When receiver not-acknowledges the transmission ends

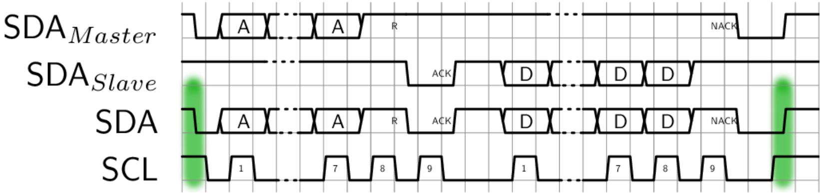
I²C Protocol Parts





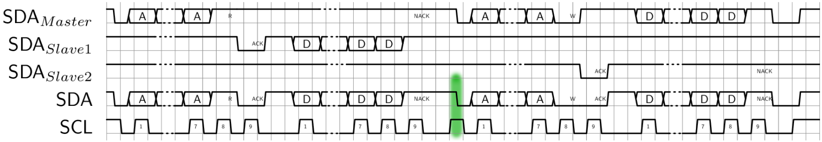
- SCL high
- Master injects Positive-going Edge on SDA

I²C Protocol Example/1

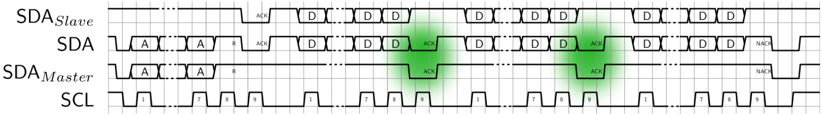


Simple I²C read on default register

I²C Protocol Example/2



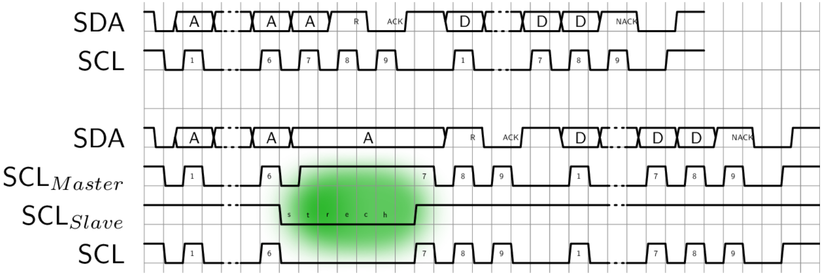
Example of repeated start



Example of multi-byte transmission

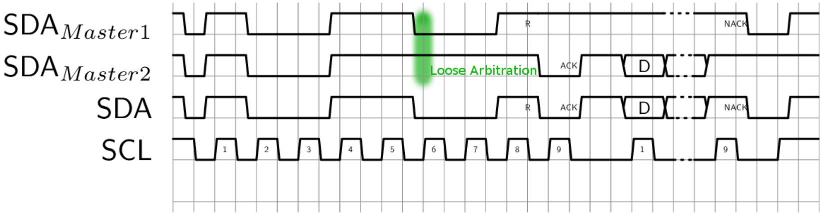
I²C Clock Stretching

- No fixed speed: Any device may slow down the transmission
- Master pauses switching of SCL →transmission is paused
- Slave holds SCL low →master waits for release



I²C Collision Detection & Bus Arbitration

- Two devices issue start condition →become master of the bus
- Both transmit address and possibly data
- One master sends "1", one sends "0"
- The master sending "1" notices the discrepancy between its output a
- A master that lost bus arbitration switches to slave mode



- Second master became slave before any race condition occured
- →no data loss

I^{2}C 10-bit Addressing

- 7-bit addressing means 128 addresses
- 16 addresses reserved →only 112 addresses free
- More addresses needed →10-bit-addressing:
  First byte: 11110 + first 2 bits of 10-bit address + R/W-bit
  Second byte: Remaining 8 bits of slave address
  Rest of transmission as usual

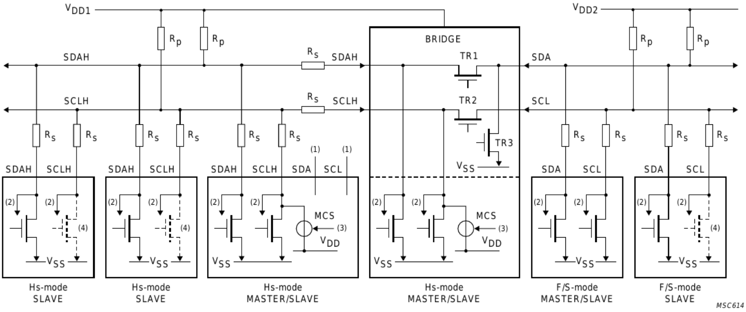


Source: Adapted from ``UM10204I2C-busspecificationandusermanualRev.6'',2014

I²C Higher Speeds

▪ Standard Mode	Up to 100kbit/s
▪ Fast Mode	Up to 400kbit/s Fully compatible with Standard Mode
▪ Fast Mode Plus	Up to 1Mbit/s Timing loosened, more drive strength
▪ High Speed Mode	Up to 3.4Mbit/s A number of changes: ◦ Pull-up current sources in each device ◦ Schmitt-trigger inputs for spike suppression ◦ Clock stretching only after `ACK` bit ◦ →special initiation: master-code "00001XX" "X" transmitted in Fast Mode Bus arbitration only during master-code transfer

I^{2}C High Speed Mode Electrical Setup



(1) Bridge not used. SDA and SCL may have an alternative function.

(2) To input filter.

(3) Only the active master can enable its current-source pull-up circuit.

(4) Dotted transistors are optional open-drain outputs which can stretch the serial clock signal SCL or SCLH.

`Source: Adapted from ``The I²C-Bus Specification v. 2.1'', 2000`

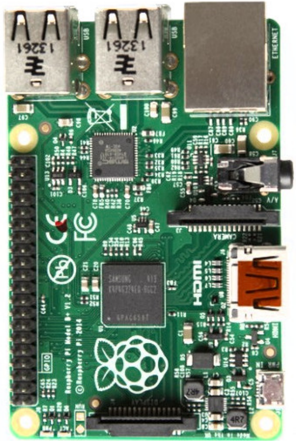
I²C Ultra Fast Mode

- Ultra Fast Mode
  Up to 5Mbit/s
  Not compatible
  Changes:
  - Unidirectional Protocol
  - Push-Pull output stages
  - Rest of protocol remains mostly the same

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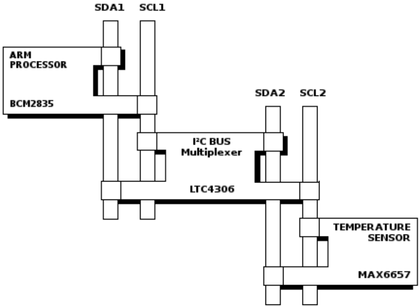
Practical Part

- Goal: Measure an I^2C transaction
- A Raspberry Pi is connected to a lab card
- Measurement done with a temperature sensor on the card



Source: http://static.trustedreviews.com/94/00002d03f/1a88_orh350w620/Raspberry-Pi-B-Plus-model.jpg

Hardware Setup



- Raspberry Pi drives I²C bus multiplexer LTC4306
- LTC4306 connected to temperature sensor MAX6657
- Oscilloscope attached to I²C bus on sensor

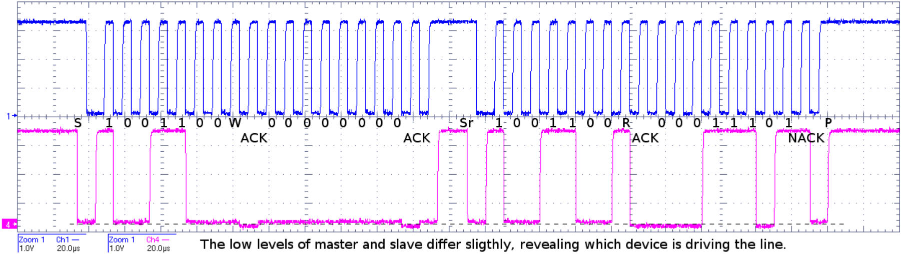
Software Setup

- Load Kernel Modules `i2c-bcm2708` & `i2c-dev`
- Load package `i2c-tools`
- Start terminal session:

Software Session

```
# Tell the multiplexer to connect the
# correct bus to the pi.
pi@raspberrypi ~ $ i2cset 1 73 3 64
WARNING! This program can confuse your
I2C bus, cause data loss and worse!
I will write to device file
/dev/i2c-1, chip address 0x49, data
address 0x03, data 0x40, mode byte.
Continue? [Y/n] y
# Read the temperature sensor.
pi@raspberrypi ~ $ i2cget -y 1 76 0
0x1b
# A thumb was placed on the sensor
# to warm it up a little
pi2@raspberrypi ~ $ i2cget -y 1 76 0
0x1d
```

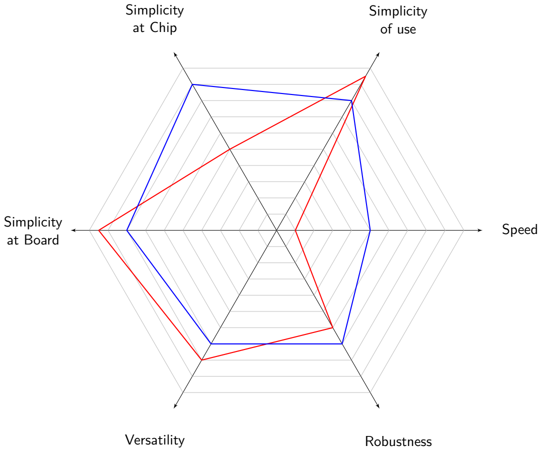
I^{2}C Measurement



The low levels of master and slave differ sligthly, revealing which device is driving the line.

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Comparison of SPI an I^2C



Comparison of the buses. (visualisation of estimation) Red: I^2C, Blue: SPI.

Conclusion

- Both SPI and I²C very mature busses
- Nevertheless up to date
- Low pin count, low speeds
- SPI used for data connections mostly
- I²C prevalently used for configuration centric communication

References

Datasheet of the Motorola MC68HC11A8 microcontroller describing the SPI bus.
Last downloaded 2014-01-10
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Last visited 2014-01-11
http://pmbus.org/about/pmbusancestry

Specification of SMBus
Last downloaded 2014-01-11
http://smbus.org/specs/smbus20.pdf

Homepage about I^{2}C detailing TWI
Last visited 2014-01-11
http://www.i2c-bus.org/twi-bus

Example of a datasheet using the term “Two Wire Interface” instead of I^{2}C
Last downloaded 2014-01-11
http://www.atmel.com/Images/2466S.pdf

End

Any Questions?